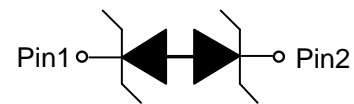


ESD5471S
1-Line, Bi-directional, Transient Voltage Suppressor
<http://www.sh-willsemi.com>
Descriptions

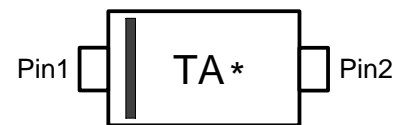
The ESD5471S is a bi-directional TVS (Transient Voltage Suppressor). It is specifically designed to protect sensitive electronic components which are connected to low speed data lines and control lines from over-stress caused by ESD (Electrostatic Discharge), EFT (Electrical Fast Transients) and Lightning.

The ESD5471S may be used to provide ESD protection up to $\pm 30\text{kV}$ (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 6A (8/20 μs) according to IEC61000-4-5.

The ESD5471S is available in SOD-523 package. Standard products are Pb-free and Halogen-free.


SOD-523 (Top View)

Circuit diagram
Features

- Reverse stand-off voltage: $\pm 5\text{V}$ Max
- Transient protection for each line according to IEC61000-4-2 (ESD): $\pm 30\text{kV}$ (contact and air discharge)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5 (surge): 6A (8/20 μs)
- Capacitance: $C_J = 9\text{pF}$ typ.
- Low leakage current
- Low clamping voltage: $V_{CL} = 12\text{V}$ typ. @ $I_{PP} = 16\text{A}$ (TLP)
- Solid-state silicon technology



TA = Device code
* = Month code (A~Z)

Marking (Top View)
Applications

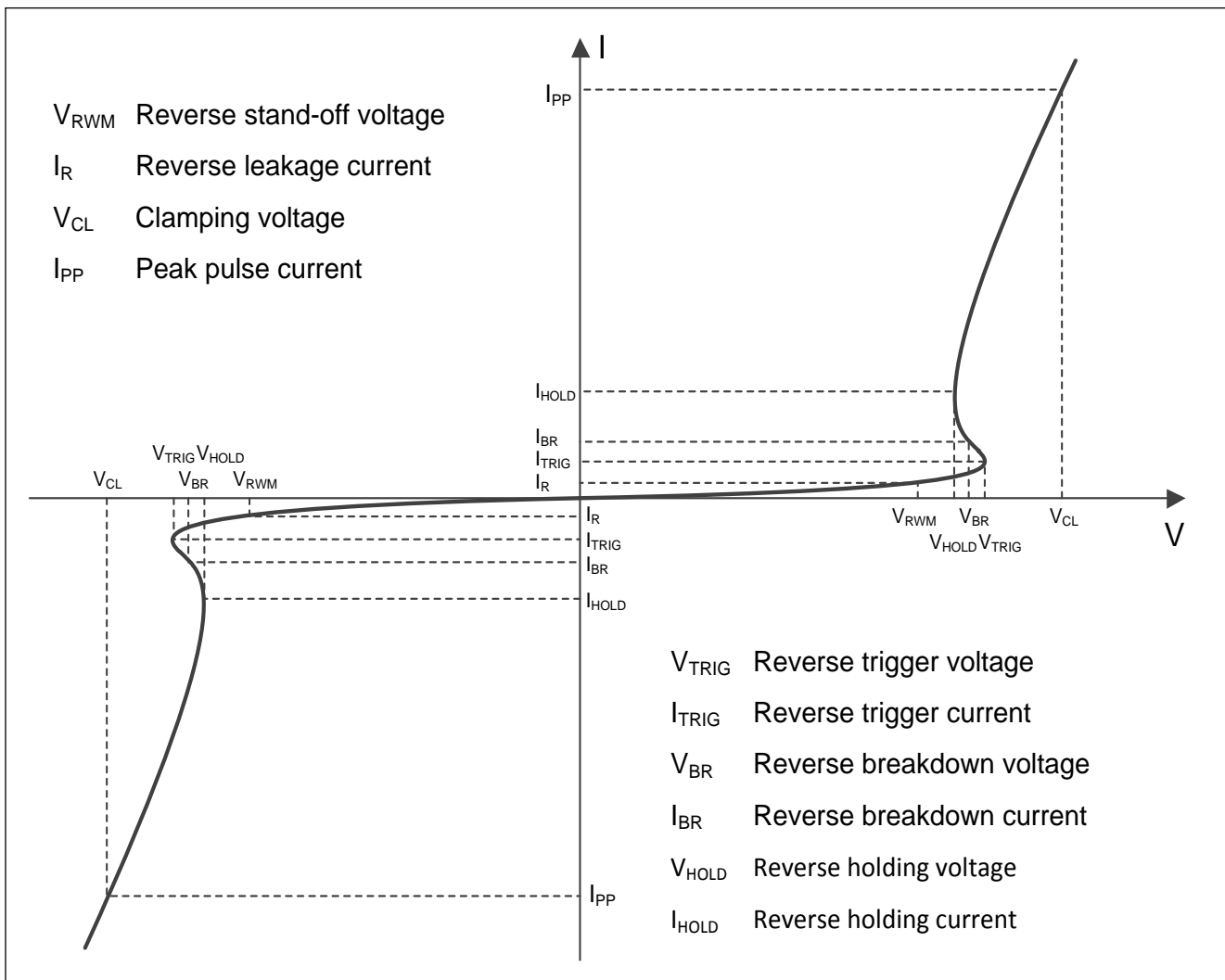
- Cellular handsets
- Tablets
- Laptops
- Other portable devices
- Network communication devices

Order information

Device	Package	Shipping
ESD5471S-2/TR	SOD-523	3000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	72	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	6	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	
Junction temperature	T_J	125	$^{\circ}C$
Operating temperature	T_{OP}	-40~85	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

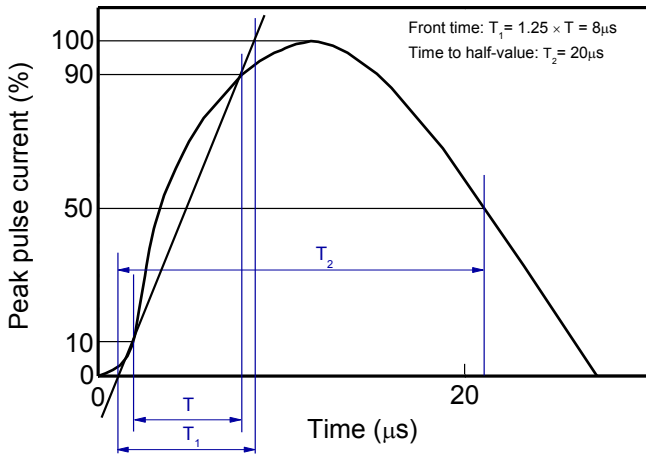
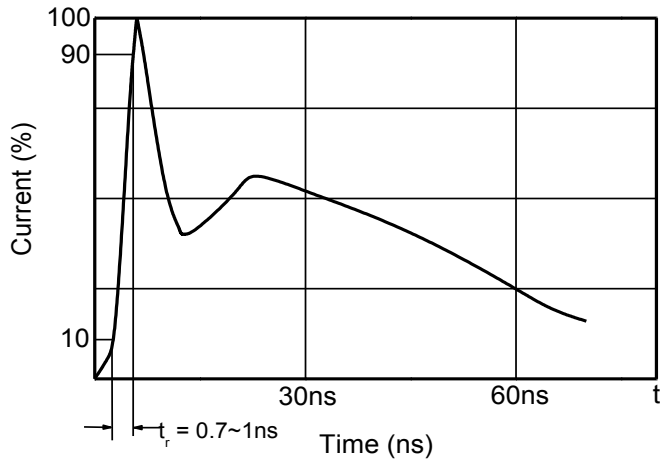
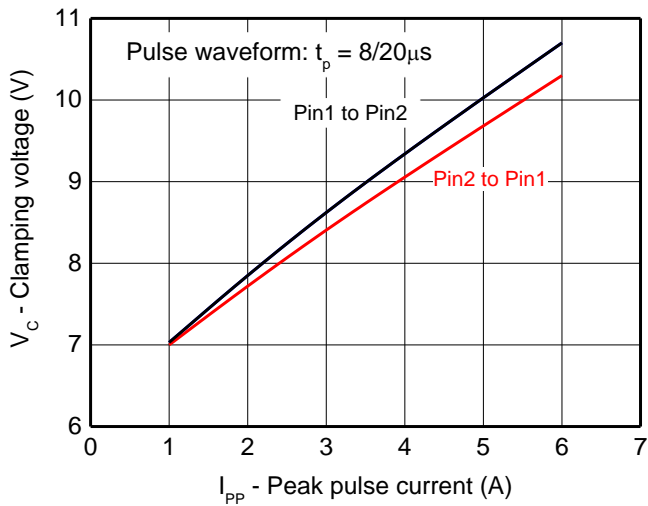
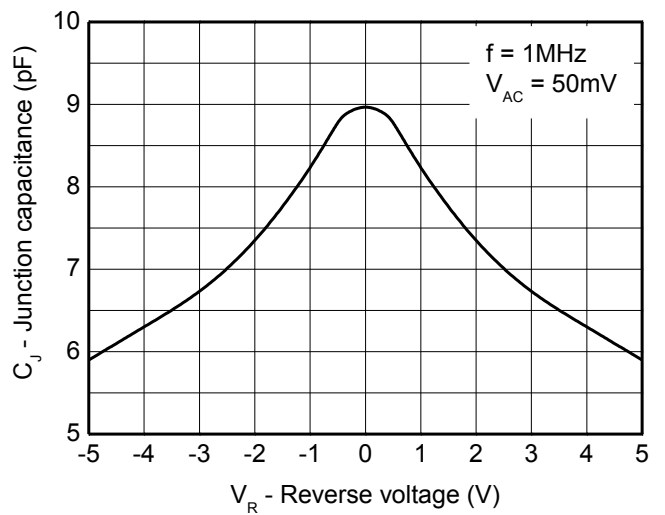
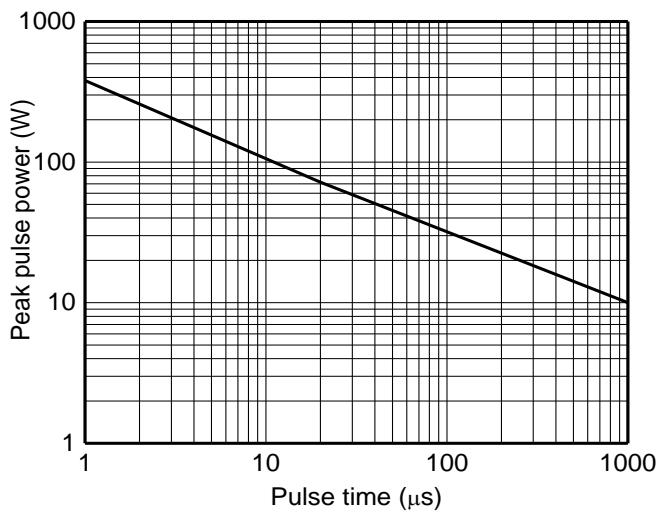
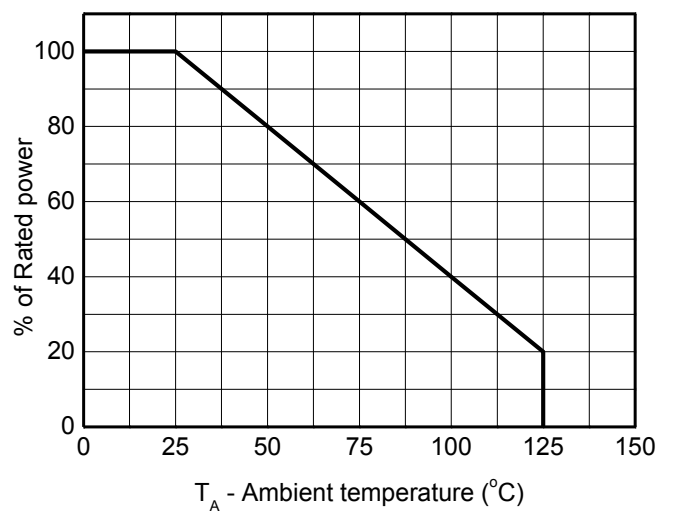
Electrical characteristics ($T_A=25^{\circ}C$, unless otherwise noted)

Definitions of electrical characteristics

Electrical characteristics (T_A=25 °C, unless otherwise noted)

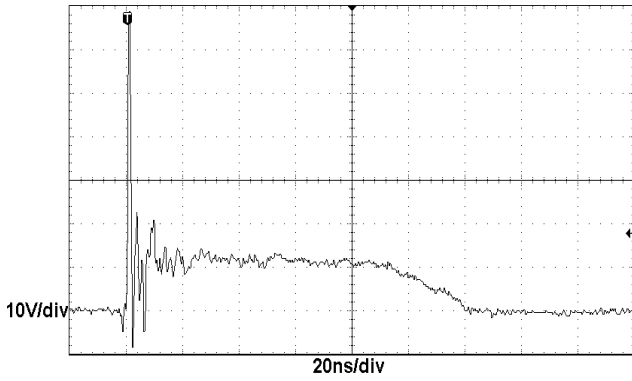
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V _{RWM}				±5	V
Reverse leakage current	I _R	V _{RWM} = 5V			1	μA
Reverse breakdown voltage	V _{BR}	I _{BR} = 1mA	5.1			V
Reverse holding voltage	V _{HOLD}	I _{HOLD} = 50mA	5.1			V
Clamping voltage ¹⁾	V _{CL}	I _{PP} = 16A, t _p = 100ns		12		V
Clamping voltage ²⁾	V _{CL}	V _{ESD} = 8kV		12		V
Clamping voltage ³⁾	V _{CL}	I _{PP} = 1A, t _p = 8/20μs			8	V
		I _{PP} = 6A, t _p = 8/20μs			12	V
Dynamic resistance ¹⁾	R _{DYN}			0.28		Ω
Junction capacitance	C _J	V _R = 0V, f = 1MHz		9	12	pF
		V _R = 5V, f = 1MHz		6	8	pF

Notes:

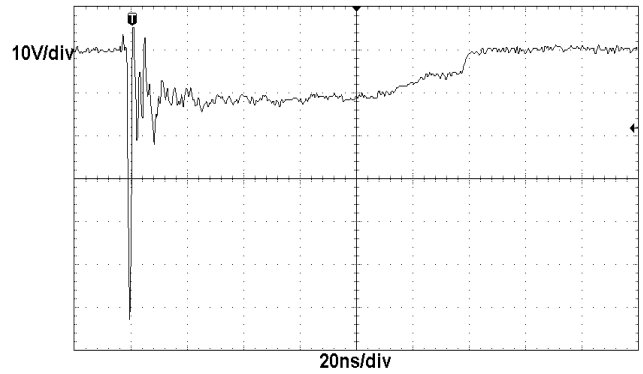
- 1) TLP parameter: Z₀ = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) Contact discharge mode, according to IEC61000-4-2.
- 3) Non-repetitive current pulse, according to IEC61000-4-5.

Typical characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

8/20 μs waveform per IEC61000-4-5

Contact discharge current waveform per IEC61000-4-2

Clamping voltage vs. Peak pulse current

Capacitance vs. Reverse voltage

Non-repetitive peak pulse power vs. Pulse time

Power derating vs. Ambient temperature

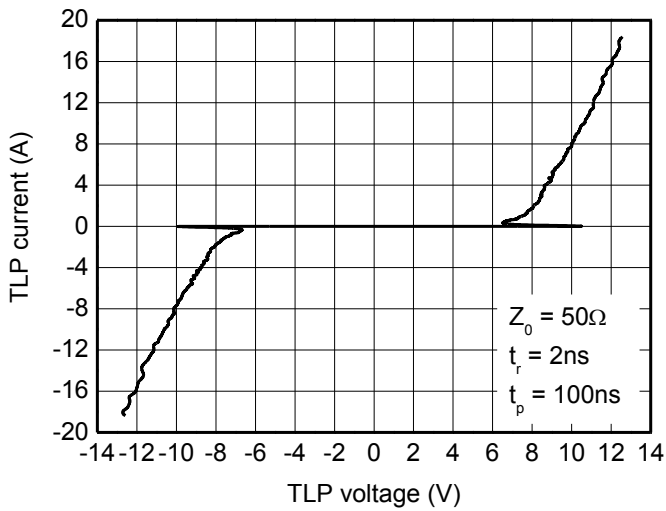
Typical characteristics ($T_A=25^{\circ}\text{C}$, unless otherwise noted)



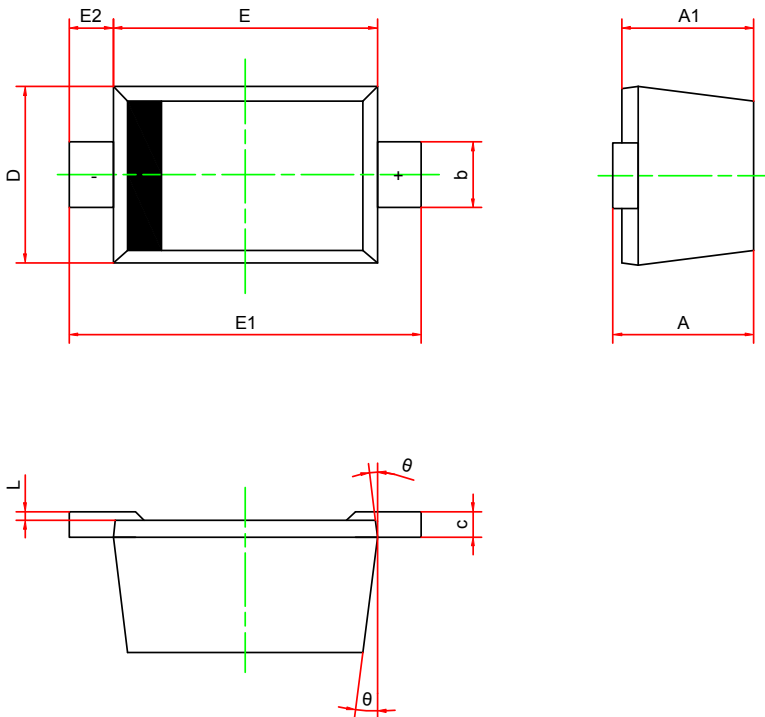
ESD clamping
 (+8kV contact discharge per IEC61000-4-2)



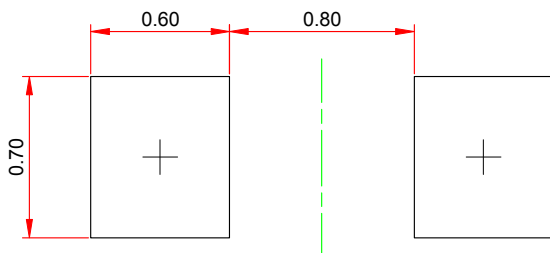
ESD clamping
 (-8kV contact discharge per IEC61000-4-2)



TLP Measurement

Package outline dimensions
SOD-523


Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	0.510	0.640	0.770
A1	0.500	0.600	0.700
b	0.250	0.300	0.350
c	0.080	0.115	0.150
D	0.750	0.800	0.850
E	1.100	1.200	1.300
E1	1.500	1.600	1.700
E2	0.200 Ref		
L	0.010	0.040	0.070
θ	7° Ref		

Recommend land pattern (Unit: mm)

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.